AMENDMENTS

DETAILED DESCRIPTION OF THE INVENTION

Please amend the Detailed Description of the Invention as follows:

Please replace paragraph [21] with the following amended paragraph:

[21] Aspects of the present invention may be found in a method and system to perform memory address translations to accomplish memory mapping for a control processor (i.e., a CPU) by way of a miniature version of a translation lookaside buffer (TLB). The miniature version of a TLB is termed a mini-TLB. The mini-TLB accomplishes odd/even page frame number translations by way of a single page frame number field instead of a dual page frame number field that is typically used in a TLB. In one embodiment, a mini-TLB facilitates the use of a decreased memory size in comparison to that used by a TLB. The address translation may be accomplished by using an existing control processor instruction set such as that provided by a MIPS control processor instruction set. In addition to using ~~a reduced~~ a TLB of reduced size, the system and method facilitates a more efficient and direct approach in performing virtual to physical memory address translation.

Please replace paragraph [26] with the following amended paragraph:

[26] Figure 3 is a relational block diagram illustrating an organizational structure of a mini-TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured

by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or ~~entry~~ the entry Lo1

register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304.

DRAWINGS

A replacement sheet is appended for Figure 1.